SysEng (S) Pte Ltd

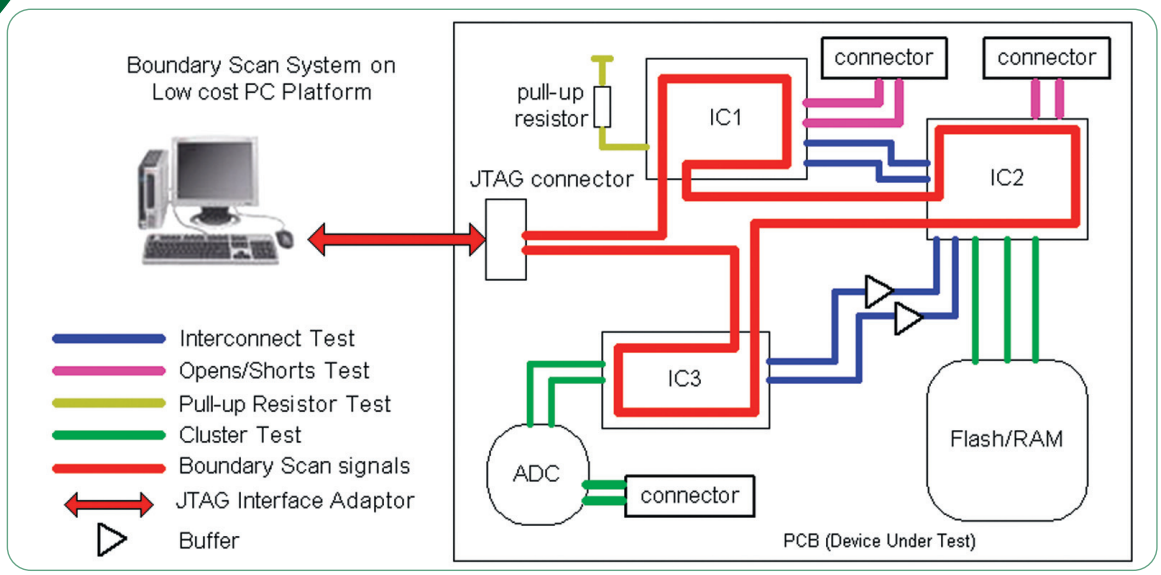
IEEE 1149.1 Boundary Scan Testing

IEEE 1149.1 Boundary Scan or widely known as JTAG is a methodology allowing complete controllability and monitoring of the boundary pins of a JTAG compatible device via software control.

Why Boundary Scan?

The industrial move to surface mount technology and multilayer boards has made testing via bed of nails system limited and inefficient. Boundary Scan test provides high test coverage for digital Printed Circuit Board and has the following advantages:

- *Overcome the constraint on the limited access of high density boards**
- *Virtual access to the board.*
- *Cost savings from not requiring fixtures in some cases.*
- *Operates on low cost PC platform.*
- *Precise fault diagnosis during manufacturing*
- *Easy integration with functional test.*
- *Automated testing controlled by Test Executive.*



Boundary Scan Test Coverage

- *ID code verification of devices.*
- *Flash Programming.*
- *Interconnect test between Boundary Scan IC chips.*
- *Open and Short-circuit test of PCB connectors.*
- *Pull-up resistor test.*
- *Perform cluster test on Non-Boundary Scan enabled devices. eg. Flash, SRAM, EPROMS, ADC, I2C devices etc.*

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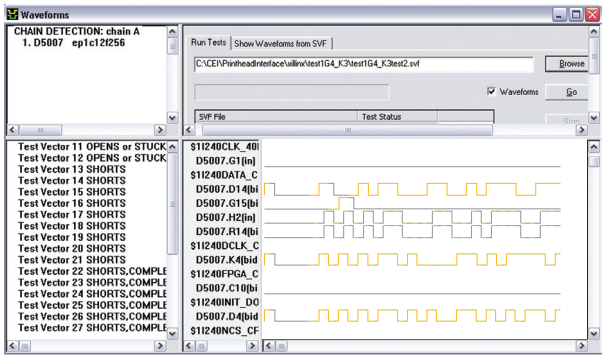
Evaluation Services

Our company provides boundary scan testability assessment for your product and customize to your testing requirements. SysEng also provide evaluation services with boundary scan development tools to verify your board design.



Customization

Customized off-line or in-line jig fixtures depending on customers testing requirements.

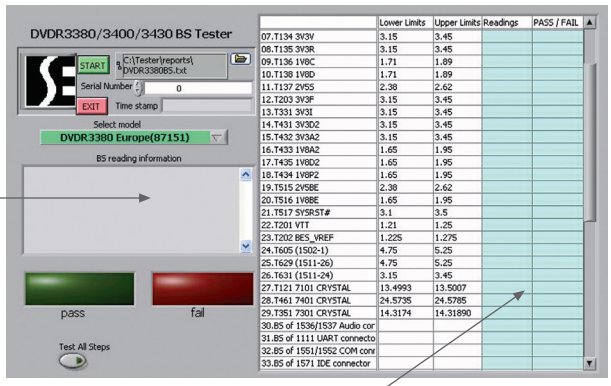
In-line Jig Fixture

Off-line Jig Fixture

JTAG Interface Adaptor

Precise Diagnosis

Diagnosis Message:
Net /VCR_DA_OUT: check for open between driver pin 7101.Y16 and pin 7101.W18.



Indicates PASS/FAIL status and measured values of each test step.

- *Easy to operate User Interface and customized report generation.*
- *Precise Diagnosis Window that pinpoint faults to pin level of IC chip that allows repairing of fault quicker than conventional way of testing.*

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